CLAIMS

What is claimed is:

1. A microelectronic package, comprising:

a heat sink;

at least one microelectronic die having an active surface and a back surface, said at least one microelectronic die back surface adjacent to said heat sink; and

an encapsulation material disposed on said heat sink and said microelectronic die active surface.

2. The microelectronic package of claim 1, further including a build-up layer disposed on an upper surface of said encapsulation material.

3. The microelectronic package of claim 2, wherein said build-up layer comprises at least one conductive trace disposed on said encapsulation material upper surface, wherein a portion of said at least one conductive trace extending through said encapsulation material to contact said at least one microelectronic die active surface.

4. The microelectronic package of claim 3, wherein said build-up layer further includes at least one dielectric layer disposed on at least a portion of the encapsulation material upper surface and said at least one conductive trace, and at least one second conductive trace extending through said at least one dielectric layer to contact said at least one conductive trace.

5. The microelectronic package of claim 1, further including a thermally conductive adhesive layer disposed between said at least one microelectronic die and said heat sink.

6. A method of fabricating a microelectronic package, comprising:

providing a heat sink;

disposing a back surface of at least one microelectronic die adjacent to said heat sink;

disposing an encapsulation material on said at least one microelectronic die and said heat sink.

7. The method of claim 6, further including forming a build-up layer on an upper surface of said encapsulation material.

8. The method of claim 7, wherein forming said build-up layer comprises forming at least one via from said encapsulation material upper surface to said at least one microelectronic die active surface and disposing at least one conductive trace on said encapsulation material upper surface, wherein a portion of said at least one conductive trace extending through said at least one via to contact said at least one microelectronic die active surface.

9. The method of claim 8, further including disposing at least one dielectric layer on at least a portion of the encapsulation material upper surface and said at least one conductive trace, forming a via through said dielectric layer, and forming at least one second conductive trace on said dielectric layer, wherein a portion thereof extends through said at least one dielectric layer to contact said at least one conductive trace.

10. A microelectronic package, comprising:

a heat sink;

a microelectronic package core having a first surface and an opposing second surface, said microelectronic package core having at least one opening defined therein extending from said microelectronic package core first surface to said microelectronic package core second surface, where said microelectronic package core second surface abuts said heat sink;

at least one microelectronic die disposed within said at least one microelectronic package core opening and adjacent said heat sink, said at least one microelectronic die having an active surface; and

an encapsulation material disposed on said microelectronic die and in portions of at least one microelectronic package core opening.

11. The microelectronic package of claim 10, further including a build-up layer disposed on an upper surface of said encapsulation material.

12. The microelectronic package of claim 11, wherein said build-up layer comprises at least one conductive trace disposed on said encapsulation material upper surface, wherein a portion of said at least one conductive trace extends through said encapsulation material to contact said at least one microelectronic die active surface.

13. The microelectronic package of claim 12, wherein said build-up layer further includes at least one dielectric layer disposed on at least a portion of the encapsulation material upper surface and said at least one conductive trace, and at least one second conductive trace extending through said at least one dielectric layer to contact said at least one conductive trace.

14. The microelectronic package of claim 11, wherein said encapsulation material covers said microelectronic package core first surface.

15. The microelectronic package of claim 10, wherein a thickness of said microelectronic package core is greater than a thickness of said at least one microelectronic die.

16. The microelectronic package of claim 10, wherein said microelectronic package core is a material selected from the group consisting of bismaleimide triazine resin based material, an FR4 material, polyimides, ceramics, and metals.

17. The microelectronic package of claim 10, further including a thermally conductive adhesive layer disposed between said at least one microelectronic die and said heat sink.

18. A method of fabricating a microelectronic package, comprising:

providing a heat sink;

disposing a back surface of at least one microelectronic die adjacent to said heat sink;

abutting a microelectronic package core adjacent said heat sink, said microelectronic package core having at least one opening defined therein extending from a first surface of said microelectronic package core to a second surface of said microelectronic package core, said at least one microelectronic die residing within said at least one microelectronic package opening;

disposing an encapsulation material on said at least one microelectronic die and in portions of at least one microelectronic package core opening.

19. The method of claim 18, further including forming a build-up layer on an upper surface of said encapsulation material.

20. The method of claim 19, wherein forming said build-up layer comprises forming at least one via from said encapsulation material upper surface to said at least one microelectronic die active surface and disposing at least one conductive trace on said

encapsulation material upper surface, wherein a portion of said at least one conductive trace extending through said at least one via to contact said microelectronic die active surface.

21. The method of claim 20, further including disposing at least one dielectric layer on at least a portion of the encapsulation material upper surface and said at least one conductive trace, forming a via through said dielectric layer, and forming at least one second conductive trace on said dielectric layer, wherein a portion thereof extends through said at least one dielectric layer to contact said at least one conductive trace.

22. The method of claim 18, wherein disposing said encapsulation material on said at least one microelectronic die and in portions of at least one microelectronic package core opening comprises disposing said encapsulation material on said at least one microelectronic die, in portions of at least one microelectronic package core opening, and said microelectronic package core first surface.

23. The method of claim 22, wherein abutting a microelectronic package core adjacent said heat sink comprises abutting a microelectronic package core, which is thicker than said at least one microelectronic die, adjacent said heat sink.

24. The method of claim 23, wherein disposing said encapsulation material on said at least one microelectronic die and in portions of at least one microelectronic

package core opening comprises disposing said encapsulation material on said at least one microelectronic die, in portions of at least one microelectronic package core opening, and said microelectronic package core first surface.

25. The method of claim 24, further including removing a portion of said encapsulation material on said microelectronic package core forming a uniform thickness of encapsulation material on said at least one microelectronic die.

26. The method of claim 25, further including forming a build-up layer on an upper surface of said encapsulation material.

27. The method of claim 26, wherein forming said build-up layer comprises forming at least one via from said encapsulation material upper surface to said at least one microelectronic die active surface and disposing at least one conductive trace on said encapsulation material upper surface, wherein a portion of said at least one conductive trace extending through said at least one via to contact said microelectronic die active surface.

28. The method of claim 27, further including disposing at least one dielectric layer on at least a portion of the encapsulation material upper surface and said at least one conductive trace, forming a via through said dielectric layer, and forming at least one

second conductive trace on said dielectric layer, wherein a portion thereof extends through said at least one dielectric layer to contact said at least one conductive trace.